REMARKS

Claims 1-4 and 9-12 have been amended. Claims 1-52 are pending in the present application. Applicants reserve the right to pursue the original claims and other claims in this application and in other applications.

After the Advisory Action, it appears that claims 1-20, 25-44 and 49-52 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Proebsting, U.S. Patent No. 5,952,948, in view of Jeong, U.S. Patent No. 6,335,721 B1 and Okada, U.S. Patent No. 5,608,421 and claims 21-24 and 45-48 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Proebsting, Jeong, Okada and Nakamura, U.S. Patent No. 6,411,273 B1. The rejections are respectfully traversed and reconsideration is respectfully requested in light of the following remarks.

The features of the claimed inventions include:

(1) A drive circuit comprising a sampling circuit. An exemplary sampling circuit is shown as reference numeral 23 in Figure 2 and reference numeral 125 in Figure 13. The main function of the claimed sampling circuits are to distribute an output voltage to a plurality of signal lines such as lines SL1-SL6 (Figure 13) and SL1-SL4 (Figure 2). Generally, many signal lines are required and e.g., 1920 lines are required for VGA resolution. If it is difficult to provide the same number of digital-to-analog conversion circuits as the number of signal lines, the number of digital-to-analog conversion circuits can be reduced to N number of signal lines, where N is an integer, by providing the claimed sampling circuit.

(2) The specification of the present application describes one of the problems with prior art systems is that a resistor ladder is increased so that power consumption is also increased (when using a resistor ladder in a digital-to-analog conversion circuit).

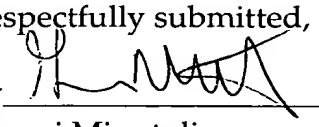
To overcome this problem, the claimed inventions utilize a drive circuit comprising a digital-to-analog conversion circuit and a sampling circuit. A voltage is divided by using a resistor in the digital-to-analog conversion circuit and a switch resistor RSW within the sampling circuit. The claimed configuration has a technical effect in that current is decreased causing power consumption to be decreased.

None of the cited prior art, even when considered in combination, teaches or suggests the claimed inventions. As such, Applicants respectfully request that the rejections be withdrawn and the claims allowed.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

Dated: February 12, 2004

Respectfully submitted,

By 

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